M64282FP Artificial Retina Technicial Information

Mitsubishi Intergrated Circuit - M64282FP - Image Sensor (Artifical Retina LSI)

1) Description

M64282FP is a 128 x 128 pixel CMOS image sensor with built-in image processing and analog image output tuning functions. This device can detect an image and process the image simultaneously as human retinas can. M64282FP can achieve smaller system size, lower power consumption, and more intelligent image processing functions.

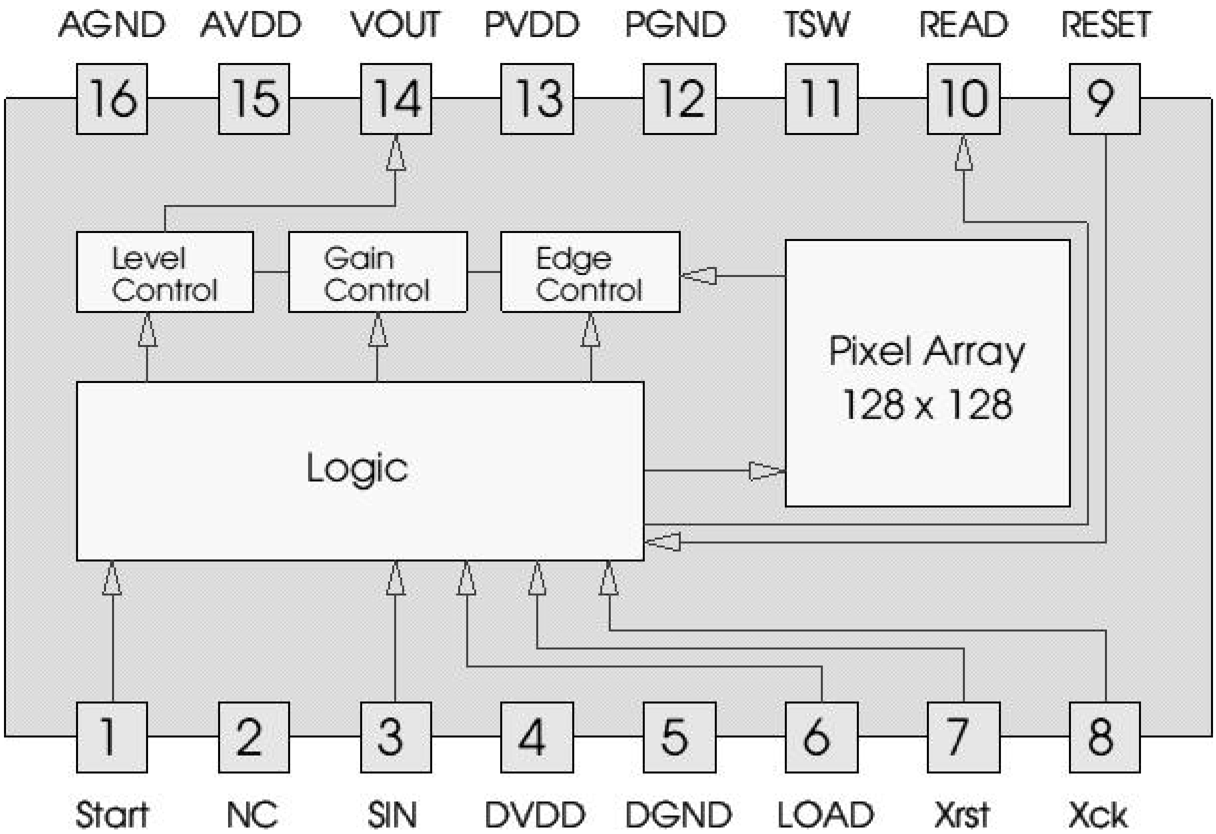
2) Features

- Single 5.0V supply
- Low power dissipation (Typ. 15 mW)
- Positive and negative image output
- Edge enhancement / extraction
- Output level & gain tuning

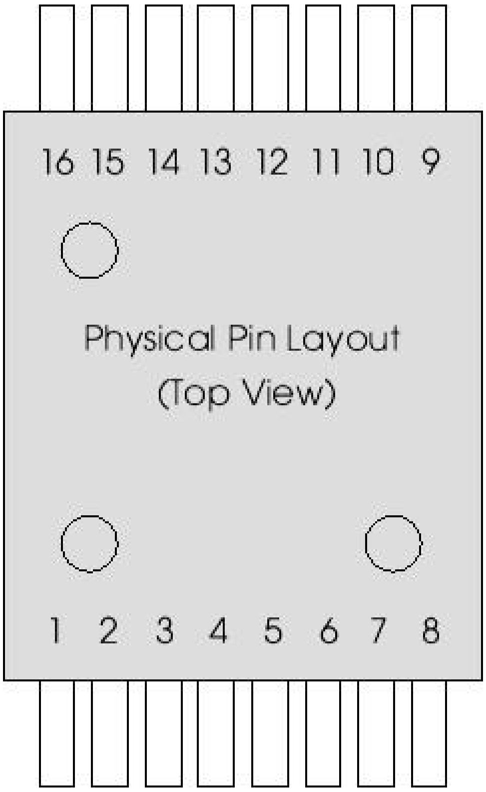
3) Application

Image input device, Gaming, Human interface for PC, etc.

4) Block Diagram



5) Pin Configuration



Pin No.	Symbol	Function	Description
1	START	Start Input	Image sensing start. Pulled down internally by 10k ohm.
2	NC		Non Connect.

3	SIN	Data Input	Parameter input. Pulled down internally by 10k ohm.
4	DVDD	Digital Power Supply	Power for logic circuits. Must be connected to 5.0V digital supply.
5	DGND	Digital Ground	Ground for logic parts.
6	LOAD	Data Set Input	Parameter set enable. Pulled down internally by 10k ohm.
7	Xrst	System Reset	System reset terminal. Pulled up internally by 10k ohm.
8	Xck	System Clock Input	Clock input MUX. Pulled down internally by 10k ohm.
9	RESET	Memory Reset Input	Parameter register reset. Pulled up internally by 10k ohm.
10	READ	Read Image	Read image signal.
11	TSW	Reserved	NOTE: Don't connect to this pin.
12	AGND1	Analog GND	Ground for analog circuits.
13	AVDD1	Analog Power Supply	Power for analog circuits. Must be connected to 5.0V analog supply.
14	Vout	Signal Output	Analog image signal output in voltage.
15	AVDD2	Analog Power Supply	Power for analog circuits. Must be connected to 5.0V analog supply
16	AGND2	Analog GND	Ground for analog circuits.

6) Image Sensing Specifications 1

Item		Specification
1	Resolution	128 x 123
2	Optical System	1/4 inch (3mm x 3mm array)

7) Image Sensing Specifications 2

Item		Specification
1	Detectable Illumination Range (Faceplate)	1 lx - 10000 lx *
2	Exposure Time Range	16 µsec - 1 sec
3	System Clock (Xck)	500 kHz
4	Frame Rate	10 fps - 30 fps
5	Output Voltage Range (Vout)	2.0 Vp-p

* Under Halogen Light Valve Illumination

8) Electrical Specifications - Absolute Maximum Ratings

Symbol	Parameter	Limits			Unit

		Min.	Typ.	Max.	
DVDD	Digital Power Supply Voltage	4.5	5.0	5.5	V
AVDD	Analog Power Supply Voltage	4.5	5.0	5.5	V

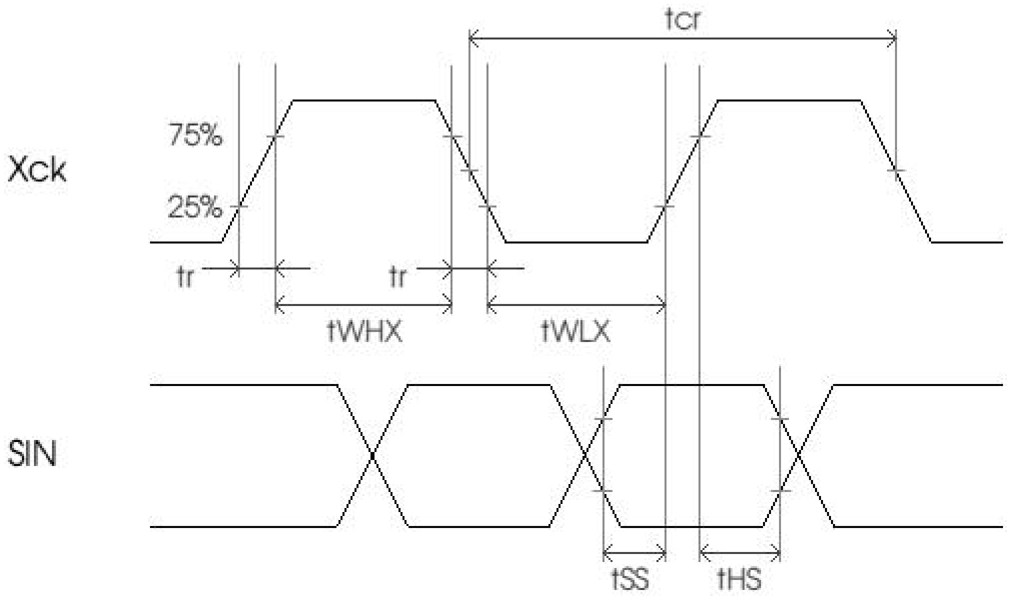
9) Electrical Specifications - DC Specifications

Symbol	**Parameter**	**Limits**			**Unit**
		Min.	Typ.	Max.	
VOH	"H" Output Voltage (READ)	4.5		DVDD	V
VOL	"L" Output Voltage (READ)	0.0		0.5	V
VIH	"H" Input Voltage	2.2		DVDD	V
VIL	"L" Input Voltage	0.0		0.8	V

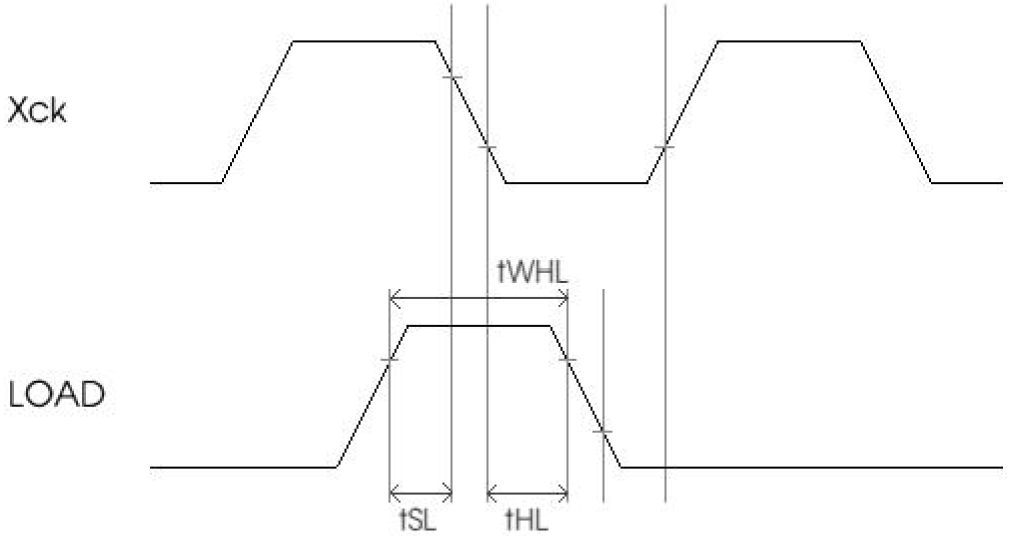
10) AC Timing Requirements

Symbol	**Parameter**	**Limits**			**Unit**
		Min.	Typ.	Max.	
tcr	Xck cycle time	2			µs
tWHX	Xck high pulse width	0.8			µs
tWLX	Xck low pulse width	0.8			µs
tr	Xck rise time			0.2	µs
tf	Xck fall time			0.2	µs
tSS	SIN setup time	0.4			µs
tHS	SIN hold time	0.4			µs
tSL	LOAD setup time	0.4			µs
tHL	LOAD hold time	0.4		tWLX-0.4	µs
tWHL	LOAD high pulse width	0.8			µs
tSXR	Xrst setup time	0.4			µs
tHXR	Xrst hold time	0.4			µs
tSR	RESET steup time	0.4			µs
tHR	RESET hold time	0.4			µs

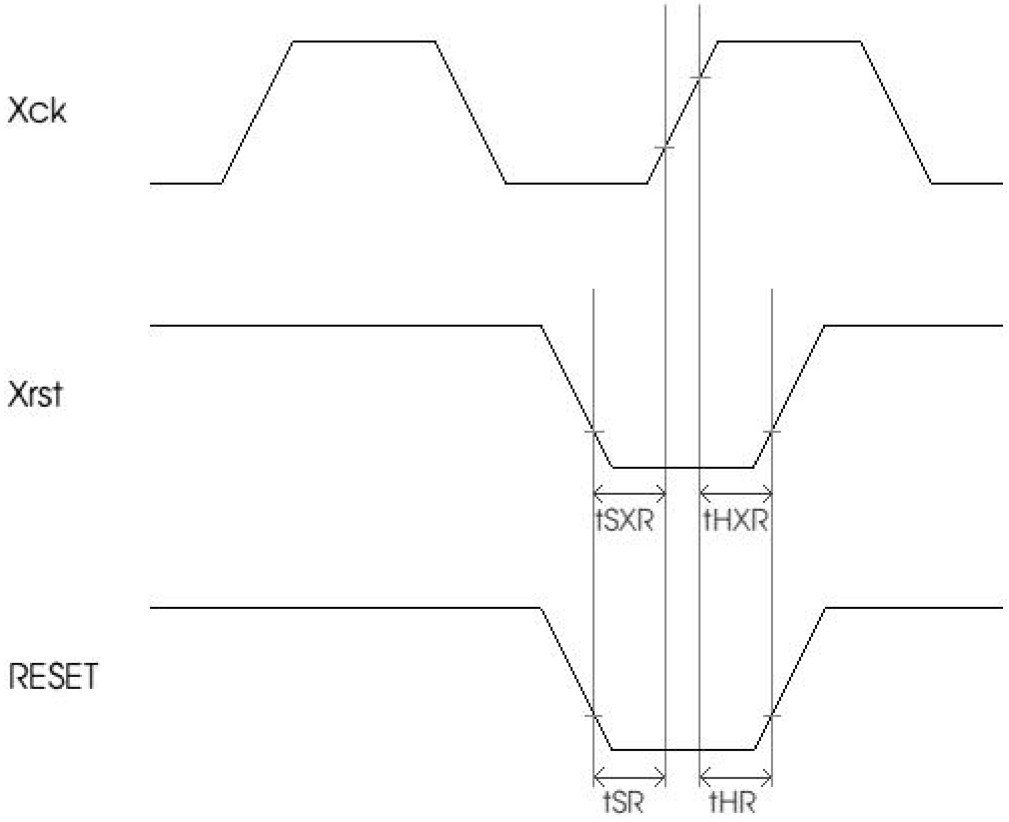
(A) Xck, SIN Timing



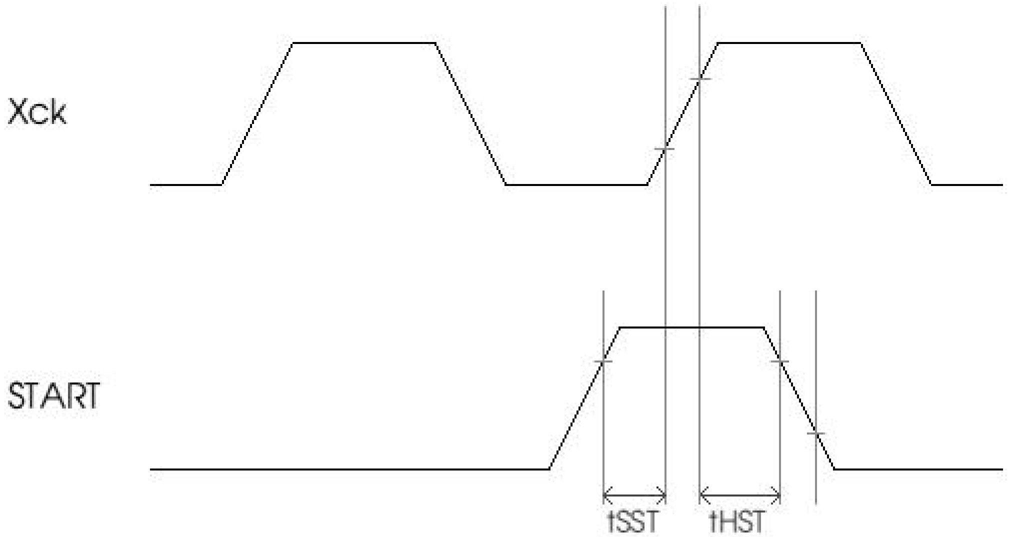
(B) Xck, LOAD Timing



(C) Xck, Xrst, RESET Timing



(D) Xck, START Timing



11) Operation

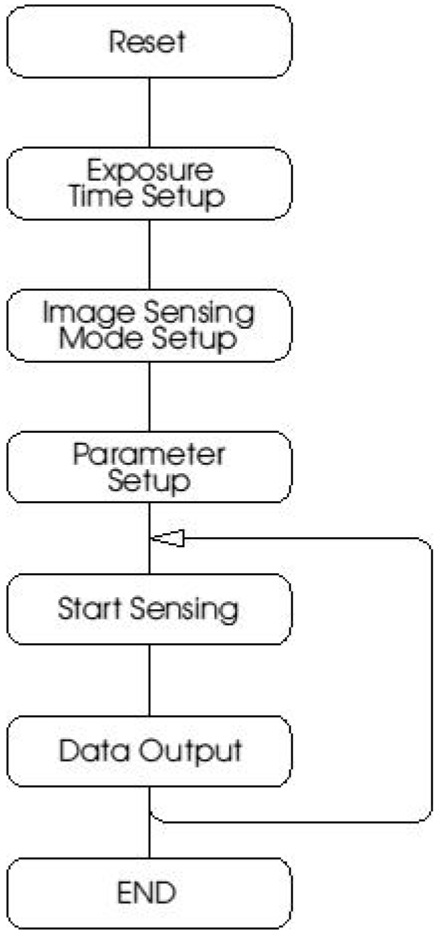


Figure 11-1 Operation Flow Chart

Figure 11-1 shows the image sensing sequence. First of all, al the registers must be reset and initialized to the appropriate values. The reset sequence completes when both Xrst and RESET signals are set low. There are 8 sets of registers, each of which consists of 8 bits of data. Each input data consists of 11 bits; of these 11 bits, the first 3 bits are the address and the last 8 bits are the data. The input data is latched at the rising edge of Xck when LOAD signal is hign, and the data of a register become valid at the falling edge of Xck.

After all register are set, START signal must be asserted. Then, image sensing sequence starts at the rising edge of Xck. Image sensing sequence consists of two different processes: the exposing process to adjust the light intensity and the image read process to put out the image data after converting optical signal into electrical signal. After the exposure time defined by the registers 2 and 3 has passed, analog image data (total 16k pixels) is read out. To read image signal, READ signal must be asserted. At this moment, it becomes possible to change the registers, because the registers are irrelevant to the image read sequence.

Once image sensing sequence starts, the chip will continue to put out image data until it is reset.

11.1) Parameter Register Assignments

Symbol	Bit Assignment	Operation
N	1 bit	Exclusively set edge ehancement mode
VH	2 bits	Select vertical - horizontal edge operation mode
E	4 bits	Edge enhancement ratio

Z	2 bits	Zero point calibration (Set the dark level output signal to Vref)
I	1 bit	Select inverted/non-inverted output
C0,C1	8 bits x 2	Exposure time
O	6 bits	Output reference voltage (in both plus and minus direction)
V	3 bits	Output node bias voltage (Vref)
G	5 bits	Analog output gain
P, M, X	8 bits x 3	1-D filtering kernal

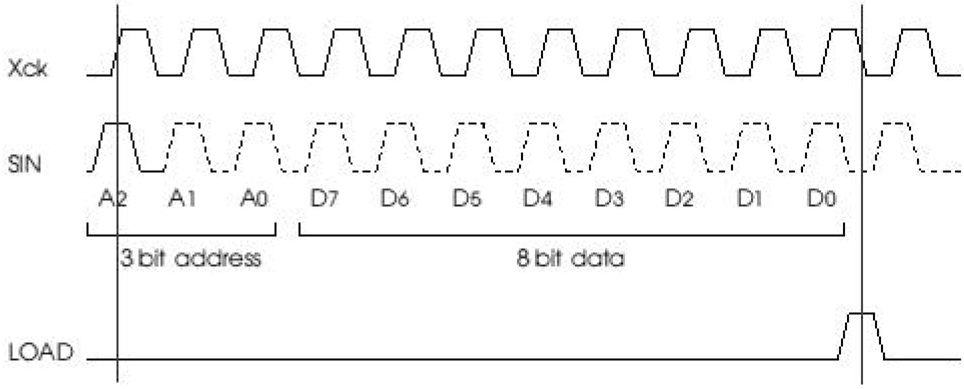
11.2) Image Acquisition Modes

Desired Mode		Action
(a)	Positive Image	Set "P" Register
(b)	Negative Image 1	Set "I" Register
(c)	Negative Image 2	Set "M" Register
(d)	Edge Extraction (V,H,2-D)	Set "N" and "VH" Register
(e)	Edge Extraction (1-D)	Set "P" and "M" Register
(f)	Edge Enhancement	Set "N", "VH" and "E" Register
(g)	Offset Level Output	Set "O" to both "C0" and "C1"

11.3) Register Assignment

Reg. No.	Address	7	6	5	4	3	2	1	0
1	001	N	VH_1	VH_0	G_4	G_3	G_2	G_1	G_0
2	010	$C1_7$	$C1_6$	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$
3	011	$C0_7$	$C0_6$	$C0_5$	$C0_4$	$C0_3$	$C0_2$	$C0_1$	$C0_0$
4	100	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
5	101	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0
6	110	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
7	111	E_3	E_2	E_1	E_0	I	V_2	V_1	V_0
0	000	Z_1	Z_0	O_5	O_4	O_3	O_2	O_1	O_0

11.4) Data LOAD sequence



11.5) About the image processing functions

Artificial retina chip can put out positive, negative, edge extracted, and edge enhanced image in accordace with the parameter register settings.

	M^N	
M^W	P	M^E
	M^S	

On-chip image processing is done with the 3 x 3 neighboring pixels. This chip executes subtraction between the central pixel P and the four neighboring pixels M^N, M^S, M^W, and M^E (see the right figure) to realize edge extraction. Moreover, this chip can program the weight of the central pixel P and the other four pixels to produce edge enhanced images.

Edge Modes	Output Signal	Effective Pixels
V-Edge Extraction	{2P-(MN+MS)}x α P-MS	128(H) x 121(V) 128(H) x 123(V)
H-Edge Extraction	{2P-(MW+WE)}x α	128(H) x 123(V)
2D-Edge Extraction	{4P-(MN+MS+ME+MW)}x α	128(H) x 121(V)
V-Edge Enhancement	P+{2P-(MN+MS)}x α	128(H) x 121(V)
H-Edge Enhancement	P+{2P-(MW+ME)}x α	128(H) x 123(V)
2D-Edge Enhancement	P+{4P-(MN+MS+ME+MW)}x α	128(H) x 121(V)

α is the edge enhancement ratio set by the "E" register.
P and M indicate the signal value from each pixel.

11.6) Register Descriptions

11.6.1) "N" register (1 bit)

If the "N" register is set, P and M registers (see 11.6.11) are exclusively set to a specific vertical edge extraction/enhancement mode. In the case of "H", for example, P register is set to 02 (HEX), and M register is set to 05 (HEX). If "N" register is set, access to P and M registers is always ignored.

11.6.2) "VH" register (2 bits)

The "VH" register selects vertical, horizontal, and 2-dimensional edge extraction/enhancement operation.

Register Setting		Edge Mode
VH_1	VH_0	
0	0	No edge operation
0	1	Horizontal edge mode
1	0	Vertical edge mode
1	1	2-D edge mode

11.6.3) "E" register (4 bits)

The "E" register sets the edge enhancement ratio α. The most significant bit E3 specifies edge enhancement mode or edge extraction mode: "H" for edge exctraction mode and "L" for edge enhancement mode (in the case of normal image sensing operation, E3 should be set low). The ratio α is set as follows. 100% means the same level as the P signal, which is the signal of the central pixel in the 3x3 processing kernal.

Register Setting			Edge Enhancement Ratio
E_2	E_1	E_0	
0	0	0	50%
0	0	1	75%
0	1	0	100%
0	1	1	125%
1	0	0	200%
1	0	1	300%
1	1	0	400%
1	1	1	500%

11.6.4) "Z" register (2 bits)

It calibrates the zero value by setting the dark level output signal to Vref.

Register Setting		Calibration
Z_1	Z_0	
0	0	No calibration
1	0	Calibration for positive signal
0	1	Calibration for negative signal

11.6.5) "I" register (1 bit)

If the "I" register is set to "H", the output signal is inverted. If is set to "L", the signal is not inverted.

11.6.6) "C0 & C1" register (8 bits x 2)

Both the C0 and C1 registers determine Exposure time; the sum of the value of C0 register and that of the C1 register determines the actual exposure time.

The offset level of image output can obtained by setting both of C0 and C1 registers to 00 (the minimum exposure time). In this caes, all pixels are read out as black level (optical black). The signal output formal is the same as that of the normal output image (synchronized with the READ signal).

"C0" register (8 bits)

Register Setting	Exposure time (msec)
00 (HEX)	0
FF (HEX)	4.080

Step width	16 µsec
Step number	256

"C1" register (8 bits)

Register Setting	Exposure time (msec)
00 (HEX)	0
FF (HEX)	1044.5

Step width	4.096 msec
Step number	256

Notice: In the case of vertical edge extraction/enhancement mode, the exposure time should be greater than 0.768 msec.

11.6.7) "O" register (6 bits)

The "O" register adjusts the offset level of the signal voltage. The most significant bit O_5 is the sign bit: "H" for plus direction, "L" for minus direction modulation. The offset is adjusted by 5 bit accuracy. The maximum absolute value of the offset level is 1V.

(In the case O_5 is "H")

Register Setting	Offset voltage (V)
20 (HEX)	0
3F (HEX)	1

Step width	32mV
Step number	32

(In the case O_5 is "L")

Register Setting	Offset voltage (V)
00 (HEX)	0
1F (HEX)	-1

Step width	-32mV
Step number	32

11.6.8) "V" register (3 bits)

It sets the output node voltage Vref.

Register Setting			Vref (V)
V_2	V_1	V_0	
0	0	0	0.0
0	0	1	0.5
0	1	0	1.0
0	1	1	1.5
1	0	0	2.0
1	0	1	2.5
1	1	0	3.0
1	1	1	3.5

11.6.9) "G" register (5 bits)

The "G" register sets the output gain of the image output signal. If the most significant bit is "H", the total gain increases by 6dB.

Register Setting				Total Gain (dB)	
				G_4	
G_3	G_2	G_1	G_0	0	1
0	0	0	0	14.0	20.0
0	0	0	1	15.5	21.5
0	0	1	0	17.0	23.0
0	0	1	1	18.5	24.5
0	1	0	0	20.0	26.0
0	1	0	1	21.5	27.5
0	1	1	0	23.0	29.0
0	1	1	1	24.5	30.5
1	0	0	0	26.0	32.0
1	0	0	1	29.0	35.0
1	0	1	0	32.0	38.0
1	0	1	1	35.0	41.0
1	1	0	0	38.0	44.0
1	1	0	1	41.0	47.0
1	1	1	0	45.5	51.5
1	1	1	1	51.5	57.5

11.6.10) Typical register settings

The following table shows the typical image acquisition modes and the register settings for each mode.

Mode	Z_1	Z_0	N	VH_1	VH_0	P	M	X	E_3	I
Posi.	1	0	0	0	0	01	00	01	0	0
Inv.	1	0	0	0	0	01	00	01	0	1
H Enh.	1	0	0	0	1	01	00	01	0	0
H Enh. Inv.	1	0	0	0	1	01	00	01	0	1
H Ext.	0	0	0	0	1	01	00	01	1	0
H Ext. Inv.	0	0	0	0	1	01	00	01	1	1
V Enh.	1	0	1	1	0	01	00	01	0	0
V Enh. Inv.	1	0	1	1	0	01	00	01	0	1
V Ext.	0	0	1	1	0	01	00	01	1	0
V Ext. Inv.	0	0	1	1	0	01	00	01	1	1
2D Enh.	1	0	1	1	1	01	00	01	0	0
2D Enh. Inv.	1	0	1	1	1	01	00	01	0	1
2D Ext.	0	0	1	1	1	01	00	01	1	0
2D Ext. Inv.	0	0	1	1	1	01	00	01	1	1

11.6.11) P and M register settings for programmable 1-D filtering

Both P and M registers specify 1-D filtering kernel consisting of +1, 0, and -1 weight values. The kernel is processed with the image pixels along vertical direction.

The following table shows the typical image acquition modes and the register settings. Some modes are the same as those of the table in 11.6.10. Moreover, "Negative" output in the table is the same as the "inverted" output in 11.6.10. V(PM) mode works similar to the filtering pattern of (+1,-1).

Mode	Z_1	Z_0	N	VH_1	VH_0	P	M	X	E_3	I
Posi.	1	0	0	0	0	01	00	01	0	0
Neg.	0	1	0	0	0	01	00	01	0	1
V (PM)	0	0	0	0	0	01	02	01	0	0
V Enh.	1	0	0	1	0	02	05	01	0	0
V Ext.	0	0	0	1	0	02	05	01	1	0
2D Enh.	1	0	0	1	1	02	05	01	0	0
2D Ext.	0	0	0	1	1	02	05	01	1	0

12) Operation Timing

(1) Chip Reset

Reset timing of the chip. Reset timing is synchronized with the rising edge of Xck clock.

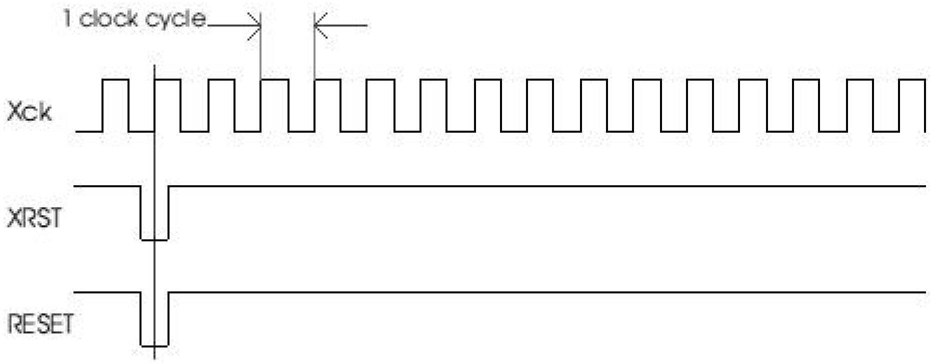
(2) Data Input

Settings of the exposure time, initial value of each scanner, Vref value, and gain value. Data (8 bits x 8) input timing is synchronized with the rising edge of Xck clock.

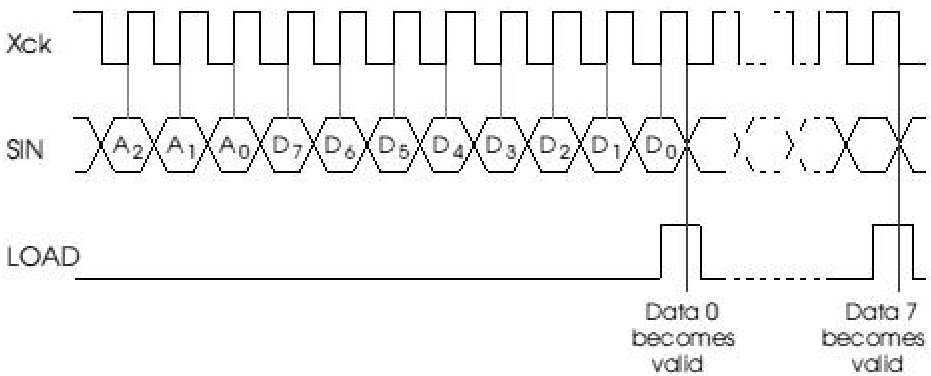
(3) Image Data Output

Image pixel data is serially read out synchronized with Xck clock.

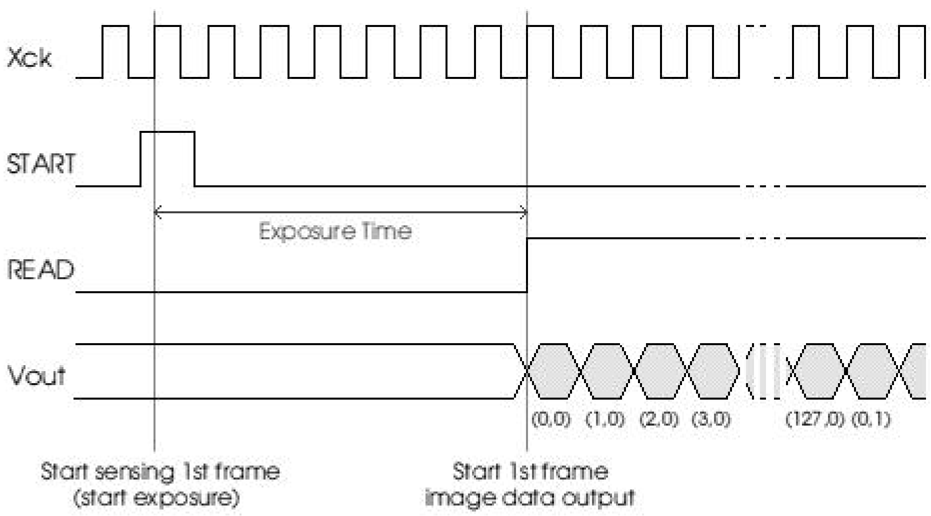
(1) Chip Reset

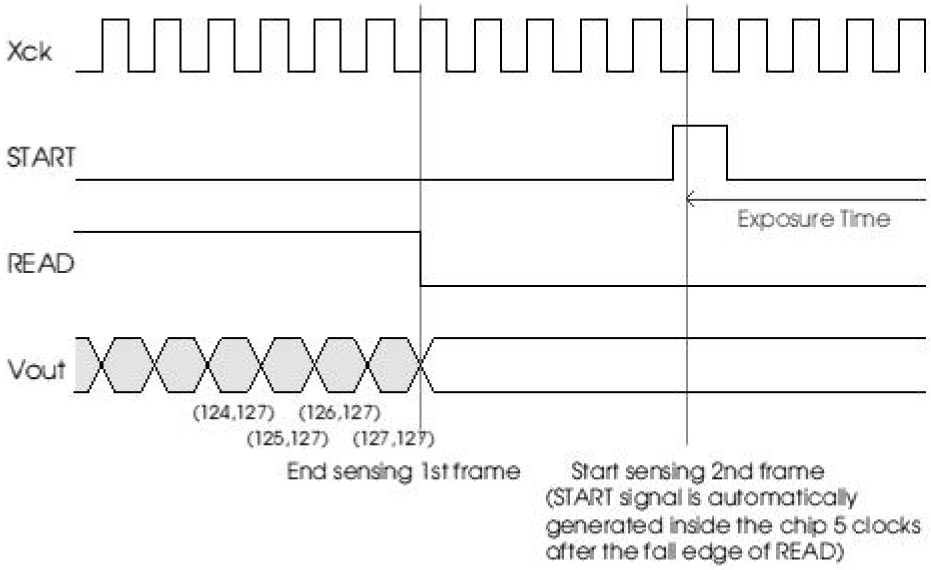


(2) Data Input



(3) Image Data Output




Xck
START
READ
Vout
Exposure Time
(124,127)
(126,127)
(125,127)
(127,127)
End sensing 1st frame
Start sensing 2nd frame
(START signal is automatically generated inside the chip 5 clocks after the fall edge of READ)