ψNAM for Massive Neuronal Assembly Modeling: Part I, Processing Elements

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Abstract. The title ψNAM stands for Parallel SImulation (PSI) for Neuronal Assembly Model(NAM). An instruction driven NAM processor [1] architecture had been proposed to model a complex stochastic neuronal assembly, capable of modeling a wide class of neuronal models including the stochastic model proposed in [2]. However, modeling the neuronal assembly using this processor will be computationally inefficient as it does not include special functional units to model the signal processing characteristics of complex dendritic tree structure. This paper proposes two processor architectures: one based on mixed signal approach - the Mixed signal NAM (MNAM) processor,and the other based on digital approach - the Digital Dendritic NAM (DDNAM) processor. In reality, modeling the complex brain functions and its fault simulation demands enormous computational resources beyond the number crunching capability of either a single MNAM or a single DDNAM processor. The companion paper, Part-II proposes a novel array architecture to meet this end.

1 Introduction

Several analog VLSI designs have been proposed to model a biological neuronal assembly. These designs assume deterministic and point source models for the neurons. However, in reality the neuronal assemblies are of stochastic nature and the neurons have finite dimensions. In this context, a novel instruction driven NAM processor[1] architecture had been proposed to model a complex stochastic neuronal assembly. NAM[1] is a general-purpose processor in the sense that it can model a wide class of neuronal models including the neuronal model proposed by Gopinath Kallianpur [2] - wherein a neuron cell is considered as a thin linear cable upon which the Wiener process is imposed. However, the NAM processor[1] does not include specific functional units to model the very important feature - the connectivity within and across the neuronal assemblies. This connectivity is established through complex dendritic tree structures. They receive vast bulk of cell's synaptic input and sum them up sub-linearly which goes as input to the soma. For some neuron types, spatially extended dendritic trees exist to provide space for a large number of quasi-independent dendritic compartments where the synaptic input to each compartment is boosted by an expansive non-linearity[7]. The absence of a specific functional unit for modeling the dendrites in the NAM processor[1] puts it at a great disadvantage when it is required to simulate a neuronal conglomeration having thousands of interconnected neurons.

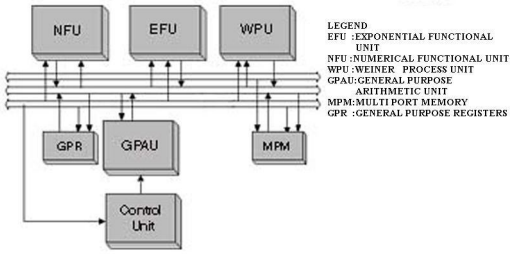

Figure 1: NAM processor.

This paper, Part-I proposes two processor architectures-

- based on mixed signal approach - the Mixed signal NAM (MNAM) processor
- based on digital approach - the Digital Dendritic NAM (DDNAM) processor

both evolved from the NAM processor [1]. The motivation for presenting two different architectures is for providing a balance between cost, performance and application needs.

In mixed signal model, custom-fabricated interconnects are used to realize the RC model of the dendrites and the MNAM processor models the soma-axon portion. In the digital model (DDNAM), an additional functional unit is integrated into the NAM processor[1] to incorporate dendritic tree modeling.

Biologically realistic simulation necessitates modeling of hundreds of thousands of neurons with dendrites. Such simulation requires an array of DDNAM

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or MNAM processors. This paper and the companion paper, Part-II ushers in Deep Sub Micron (DSM) technology into the realm of simulation and modeling of biological neuronal assembly. Such arrays can be used for fault simulation, modeling the functionality of visual or auditory cortex and eventually the Brain itself.

The following section deals with modeling of dendrites which includes discussions on existing analog modeling of dendritic tree, mixed signal modeling and digital modeling. Section 3 contains the simulation results and the comparative analysis of proposed models.

2 Modeling of Dendritic Trees

2.1 Existing Analog Modeling of Dendritic Tree

In present analog VLSI models, the dendritic tree is modeled as a multibranched, passive cable structure with multiple synaptic sites as in Silicon Neuromorph [3]. The core argument favoring analog VLSI is that it has much better fault tolerance and lesser device count. However, speed, programmability, stability with respect to temperature and noise immunity are poor for realistic simulation of a neuronal conglomeration. Additionally, the packing density of devices is lesser which results in wastage of area.

2.2 Mixed Signal Modeling

To overcome the problem associated with a fully analog based implementation, the dendrites are modeled as analog, and a Mixed signal Neuronal Assembly Model (MNAM) processor models the soma-axon portion. This leads to the concept of mixed signal design. The proposed architecture embracing the mixed signal domain - realizes the dendritic signal processing of the synaptic inputs, through physical interconnects which are custom fabricated. Any dendritic branch is treated as a cable having finite compartments, each modeled as an RC network (refer Fig.2). The functional units of the MNAM processor are serial and operate at low clock frequencies as it simulates only a single neuron (refer Fig.7). As the interconnects also conform to the lossy transmission line model (cable theory), the dendritic processing is mapped onto them. Here the interconnect dimensions are so varied to match the R and C values of the dendrites. This exactly models the variations in the signal characteristics of any synaptic input with distance and time. This can be realized in a neuronal conglomeration using interconnect based grid structure and is presented in the companion paper, Part-II.

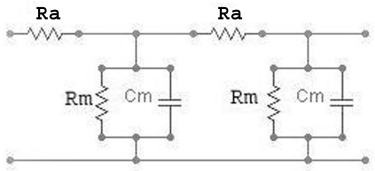

Figure 2: Dendritic tree with two quasi-independent compartment.

Mixed signal architecture needs the inclusion of Digital to Analog Converter(DAC) and Analog to Digital Converter(ADC) to the NAM processor[1]. A current source based DAC and a successive approximation ADC is employed in the model. Extensive simulations of the signal processing over the dendrites and the processing within the MNAM processor has led us to fix 11 bits for the ADC and DAC and 80 bit floating point for the processor.

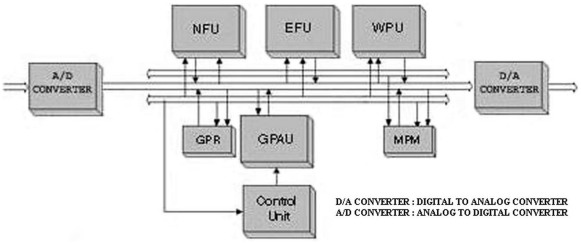

Figure 3: MNAM processor.

2.3 Digital Modeling

The programmability and the speed of the mixed signal processor is limited when simulating a neuronal conglomeration. By resorting to digital model the benefits of multi-giga hertz DSM technology can be fully utilized and this facilitates the simulation of several neurons in a single NAM processor[1]. However, the NAM processor[1] does not possess a specialized functional unit to model the dendrites so as to simulate an ensemble of neurons. Hence a special functional unit is integrated into the NAM processor[1] to model the dendrites, which leads to a new Digital Dendritic Neuronal Assembly Model (DDNAM) processor.

2.3.1 Mathematical Model of Dendrites and Method of Solution

A generic dendritic tree is shown in Fig.4. The depolarization voltages $V_{j,k}(x,t)$ of the dendrites are obtained from a system of $[2^{n+1}-1]$ Partial Differential Equations (PDEs)(refer eqn.1) where 'n' is the order of branching. The PDEs are reduced to s-domain algebraic equations by Laplace Transformation. The general solution of these PDEs and their corresponding boundary conditions at the nodes and terminals of the dendritic tree results in $2[2^{n+1}-1]$ simultaneous equations (refer eqn.2,3,4,5). These simultaneous

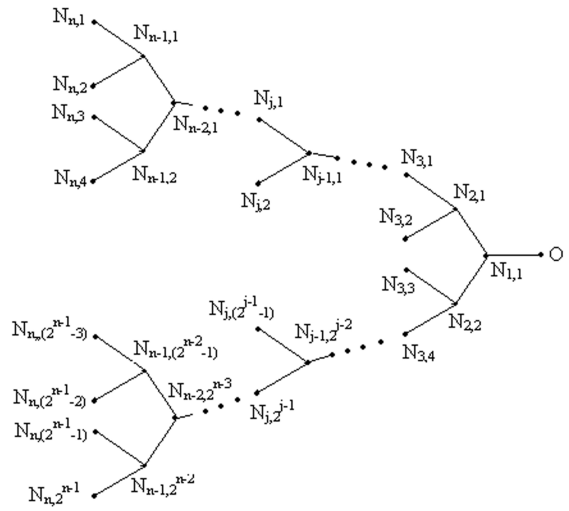

Figure 4: Notation to be employed for a complete dendritic binary tree with 'n' order of branching. $N_{j,k}$ are nodes. Each branch in the above tree having a length of $L_{j,k}$ is characterized by depolarization voltage of $V_{j,k}(x,t)$, where j=1 to n and k=1 to 2^{j-1} for each j, and O represents soma.

equations are solved by matrix methods.

$$\frac{\partial V_{j,k}(x,t)}{\partial t} = \frac{\partial^2 V_{j,k}(x,t)}{\partial x^2} - V_{j,k}(x,t) + I_{j,k}(x,t) \quad (1)$$

$$j = 1 \ldots n \quad , k = 1 \ldots 2^{j-1} \text{ for each j.}$$

and the boundary conditions are

$$\frac{\partial V_{j,k}(0,t)}{\partial x} = 0 \quad j = n, k = 1 \ldots 2^{n-1} \quad (2)$$

$$\begin{aligned} V_{j+1,2k-1}(L_{j+1,2k-1},t) &= V_{j+1,2k}(L_{j+1,2k},t) \\ &= V_{j,k}(0,t) \quad (3) \end{aligned}$$

$$\begin{aligned} \frac{1}{r_{j+1,2k-1}} \frac{\partial V_{j+1,2k-1}(x,t)}{\partial x} &+ \frac{1}{r_{j+1,2k}} \frac{\partial V_{j+1,2k}(x,t)}{\partial x} \\ &= \frac{1}{r_{j,k}} V_{j,k}(x,t) \quad (4) \end{aligned}$$

$$j = 1 \ldots n \quad , k = 1 \ldots 2^{j-1} \text{ for each j.}$$

$$\frac{\partial V_{1,1}(L_{11},t)}{\partial x} = 0 \quad (5)$$

2.3.2 Architecture

A Triangular System Solver(TSS) is used to solve the resulting matrix. The matrix method chosen for TSS is the LU decomposition. The architectural design of the functional unit for performing the LU decomposition is based on [4] to obtain $V_{11}(L_{11},s)$. To obtain the time dependent voltage an inverse Laplace transformation algorithm proposed by Zakian[6] is used. This algorithm can be executed in the GPAU of the DDNAM.

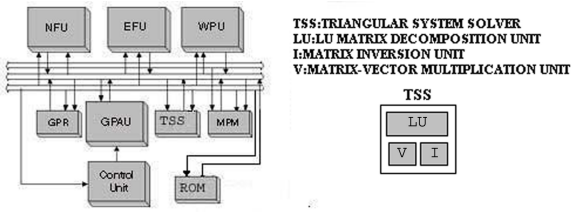

Figure 5: DDNAM processor.

Due to parallel architecture of the functional units of the DDNAM processor, it can simulate several neurons with dendritic trees (refer Fig.7). Extensive simulation of neuronal assembly was performed to determine the dynamic range of the intermediate parameter values, necessitating a 80 bit floating point DDNAM processor.

The simulation results of the DDNAM processor, and the MNAM processor along with the custom fabricated interconnect model are presented in the next section.

3 Simulation Results

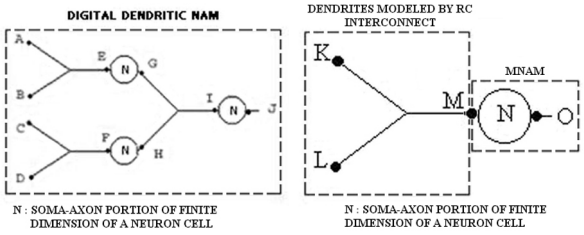

Figure 6: Simulation diagram for DDNAM, and MNAM with RC interconnects modeling the dendrites respectively.

Functional level simulation of the proposed DDNAM processor (Characteristic length of each cable(λ)=0.65cm, Internal resistance/characteristic length(R_∞) = 9750Ω, Electrotonic length of each cable=0.1539.), and the MNAM processor with RC interconnects ($R_M = 4K\Omega\ cm^2$,$R_A = 150\Omega\ cm$, $C_M = 1\mu$ F cm^{-2} (refer Fig.2), length of each compartment=0.1cm, No. of compartments/ branch=10.) was performed. A single DDNAM processor simulates the configuration shown in Fig.6 by event driven simulation. The depolarization voltage at various nodes E,F,G,H,I,J (refer Fig.9,10) for the input currents at nodes A,B,C,D (refer Fig.8) of Fig.6 are provided . The MNAM processor simulates a single neuron cell's soma-axon cable which is fed by the RC interconnects as shown in Fig.6. The depolarization voltage at various nodes M,O (refer Fig.11) for

the input voltages at nodes K,L (refer Fig.11) of the Fig.6 are provided.

4 Conclusion

Two processor architectures were proposed for modeling stochastic neuronal assembly. Unlike the NAM processor presented in [1] the proposed architecture possesses the capability to model dendritic trees. The motive behind presenting such architectures is to give a balance between cost, performance and application needs. A three neuron structure with single order branching of dendrites was simulated using the proposed DDNAM processor. In mixed signal model the MNAM processor was used to simulate the soma-axon cable of a neuron, the dendrites of single order branching were simulated using custom-designed interconnects modeling their RC network equivalent. These architectures pave the way for evolving an array processor for simulation of massive neuronal assemblies, discussed in the companion paper, Part-II.

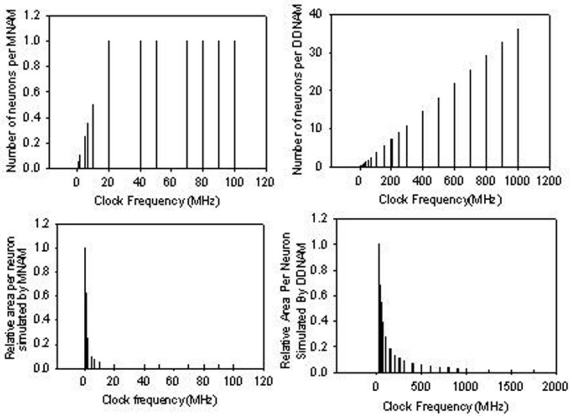

Figure 7: Comparitive analysis of Neuronal Models.

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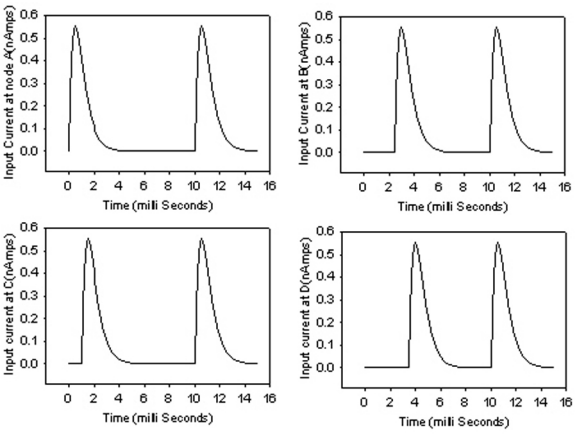

Figure 8: Input Current at node A,B,C,D.

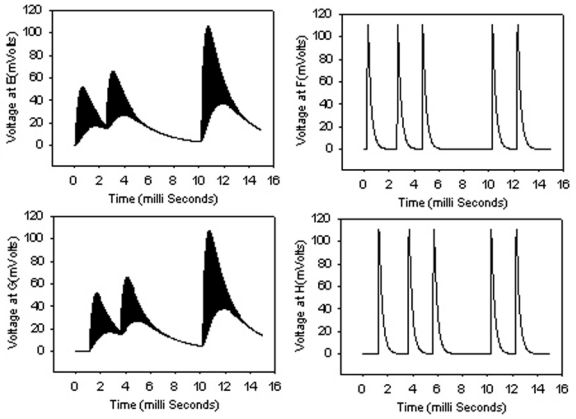

Figure 9: Depolarized Voltage at node E,F,G,H.

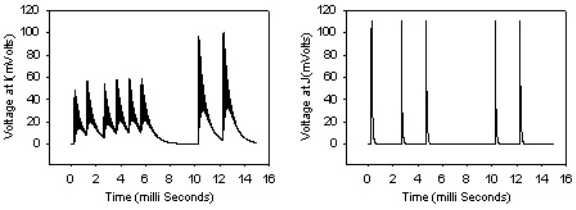

Figure 10: Depolarized Voltage at node I,J.

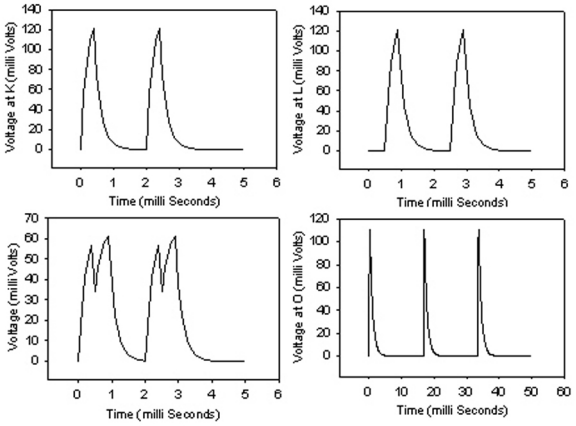

Figure 11: Depolarized Voltage at node K,L,M,O.