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HARISH BARATHVAJASANKAR

OBJECTIVE

A Position in the field of Computer Science with special interest in Computer Architecture and System Programming

EDUCATION

Bachelor of Engineering (B.E.) Expected April 2004
Computer Science and Engineering
Sri Venkateswara College of Engineering
Affiliated to University of Madras
Sriperumbudur

Aggregate till 6th Semester: 84.6%

RESEARCH AFFILIATION

Research Trainee under Prof. N.Venkateswaran 2002 onwards

Waran Research Foundation (WARF)
46 B, Mahadevan Street,
West Mambalam,
Chennai.

URL: http://warfindia.org

AWARDS RECEIVED

- Certificate of merit for standing *second* in the Department of Computer Science and Engineering in October 2002 Semester Examinations
- Intel HiPC Scholarship for High Performance Computing Conference 2004 at Hyderabad.

INTERESTS AND ACTIVITIES

- Computer Architecture
  My interest is design of novel architectures for specific applications, super computing architectures and performance analysis.

- Mapping
  Mapping of complex structures on architectures and development of models and algorithms for the same are special interests.

- Digital Signal Processing
  Design of Architectures for special purpose signal processing and low power aspects

- System Programming
  Creating novel systems for special purpose applications

- Web designing activities
  Administrator and cofounder of http://www.warfindia.org

SKILLS

- Programming Languages
  BASIC, C, C++, JAVA, ASP, Visual Basic, LaTex
- Tools
  Verilog HDL, VHDL, Neuron, Photoshop, Obj2asm
- Database
  MS Access, Oracle
- Operating Systems
  Windows, Linux, UNIX
- Troubleshooting

PROJECTS

"***KDSP1010: A Low Power DSP Architecture Design***"-Submitted to the University of Madras towards the fulfillment of the Term Paper CSE704 - Design of Computer Systems - Mini project.

"***Conceptual Evolution of DNA Processor: Computation and Control***" - Submitted to the University of Madras in partial fulfillment of the requirement for the award of the degree of Bachelor of Engineering.
Expected Completion Date: March 2004

"***Evolving MIP (Memory in Processor) based supercomputing architecture towards understanding color information encoding***" - submitted to WARF in partial fulfilment of the course.
Expected Completion Date: December 2003

PATENTS AND PUBLICATIONS

Papers Published

N Venkateswaran, R Rajesh, N Sudarshan, R Rajasimhan, C Chandramouli, R Chidambareswaran, B Harish, Kolluru Arvind, M Muhilan., *ψNAM For Massive Neuronal Assembly Modeling: Part-I, Processing Elements,* The 6th International Conference on Computational Intelligence and Natural Computing,2003.

N Venkateswaran, R Chidambareswaran, B Harish, Kolluru Arvind, R Rajesh, N Sudarshan, R Rajasimhan, C Chandramouli,*ψ NAM For Massive Neuronal Assembly Modeling: Part-II*, The Array Architectures, The 6th International Conference on Computational Intelligence and Natural Computing,2003.

Papers Under Communication

N Venkateswaran, R Chidambareswaran, B Harish, Kolluru Arvind, *An Integrated Process for Simulating the Retinal Pathway on the Special Purpose Neuronal Assembly Model Array Processor*, EHARD 2004.

N Venkateswaran, R Chidambareswaran, B Harish, Kolluru Arvind, *DNA Based Evolvable Instruction Set Architecture Arithmetic Unit*, EHARD 2004.